EE 230
Lecture 43

Data Converters

Nonideal Effects

Review from Last Time:

Engineering Issues for Using Data Converters

1. Inherent with Data Conversion Process

- Amplitude Quantization
- Time Quantization

(Present even with Ideal Data Converters)

2. Nonideal Components

- Uneven steps
- Offsets
- Gain errors
- Response Time
- Noise

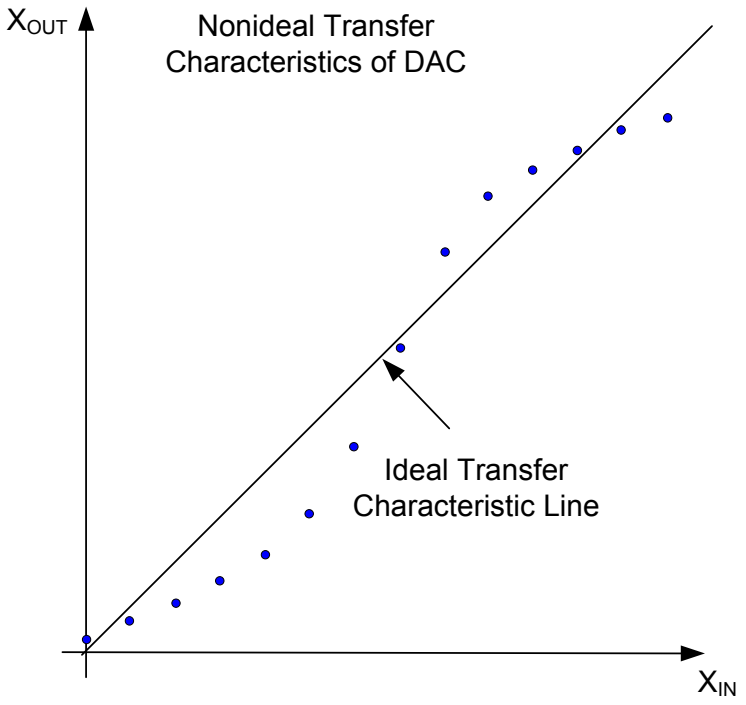
(Present to some degree in all physical Data Converters)

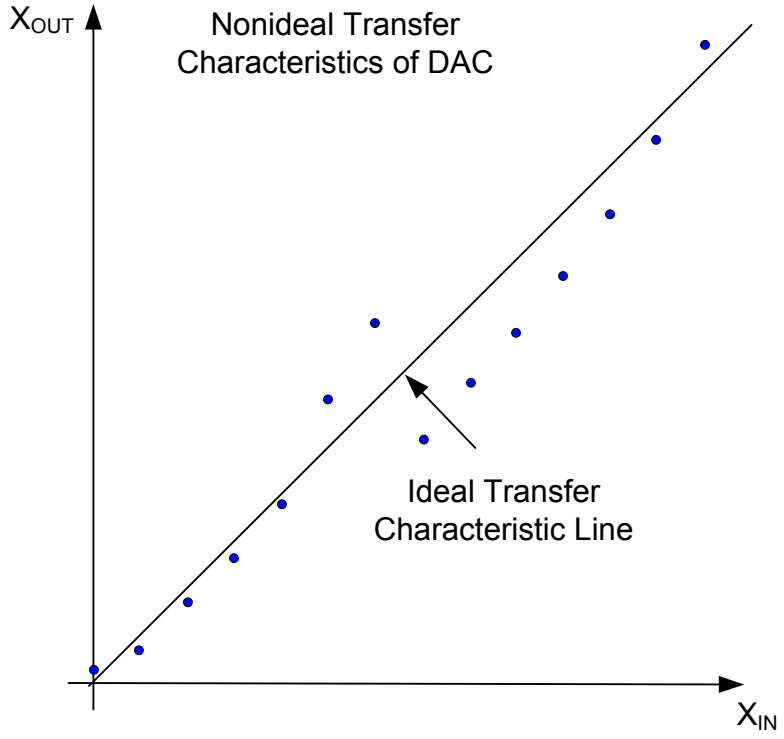
How do these issues ultimately impact performance ?

Review from Last Time:

Nonideal Transfer Characteristics

Uneven Steps



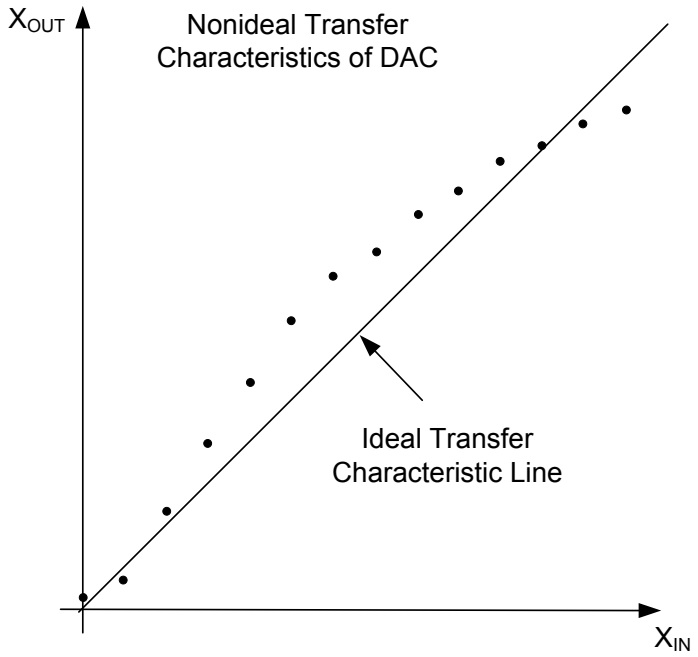


Actual transfer characteristics can vary considerably from one device to another

Review from Last Time:

Nonideal Transfer Characteristics

Uneven Steps



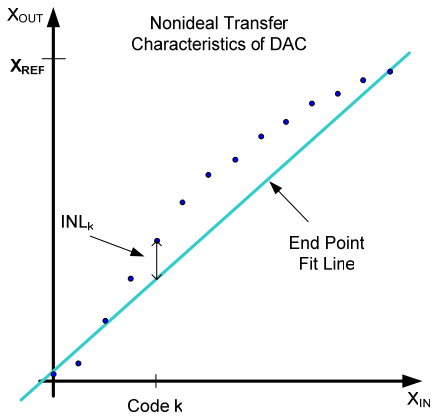
This is termed a nonlinearity in the data converter

Linearity metrics (specifications) include INL, DNL, THD and SFDR

Review from Last Time:

Integral Nonlinearity (INL)

$$INL = \max_{1 \le k \le N} \left\{ \left| INL_k \right| \right\}$$



Linearity metrics:
- INL
- DNL
- THD
- SFDR

Often expressed in LSB:

$$INL_{LSB} = \frac{INL}{X_{LSBF}}$$

where

$$X_{LSBF} = \frac{X_{OUT}(N) - X_{OUT}(1)}{N-1}$$

but

$$X_{LSBF} = \frac{X_{OUT}(N) - X_{OUT}(1)}{N-1} \cong \frac{X_{REF}}{2^n}$$

$$INL_{LSB} \cong 2^n \frac{INL}{X_{REF}}$$

Review from Last Time:

Integral Nonlinearity (INL)

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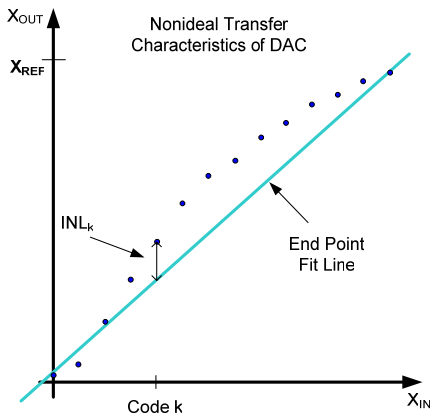
$$INL_{LSB} \cong 2^n \frac{INL}{X_{REF}}$$



Linearity metrics:
- INL
- DNL
- THD
- SFDR

What is the ideal INL?

$$INL_{IDEAL} = 0_{LSB}$$

What is an acceptable INL?

If INL<0.5LSB, it is generally considered acceptable

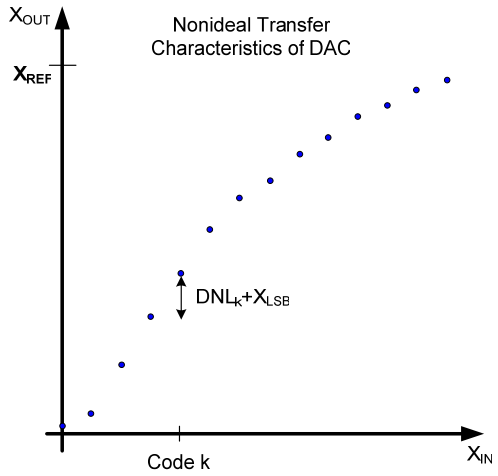
This would be the quantization error for an n-bit ADC

What is the INL of a DAC?

Varies from part to part, often close to 0.5LSB, occasionally better, but often worse - Given in Data Sheet

Review from Last Time:

Differential Nonlinearity (DNL)



Linearity metrics:
- INL
- DNL
- THD
- SFDR

$$DNL = \max_{1<k\leq N}\left\{\left|DNL_k\right|\right\}$$

$$DNL_{LSB} \cong 2^n \frac{DNL}{X_{REF}}$$

What is the IDEAL DNL of a DAC?

Ideal DNL $=0_{LSB}$

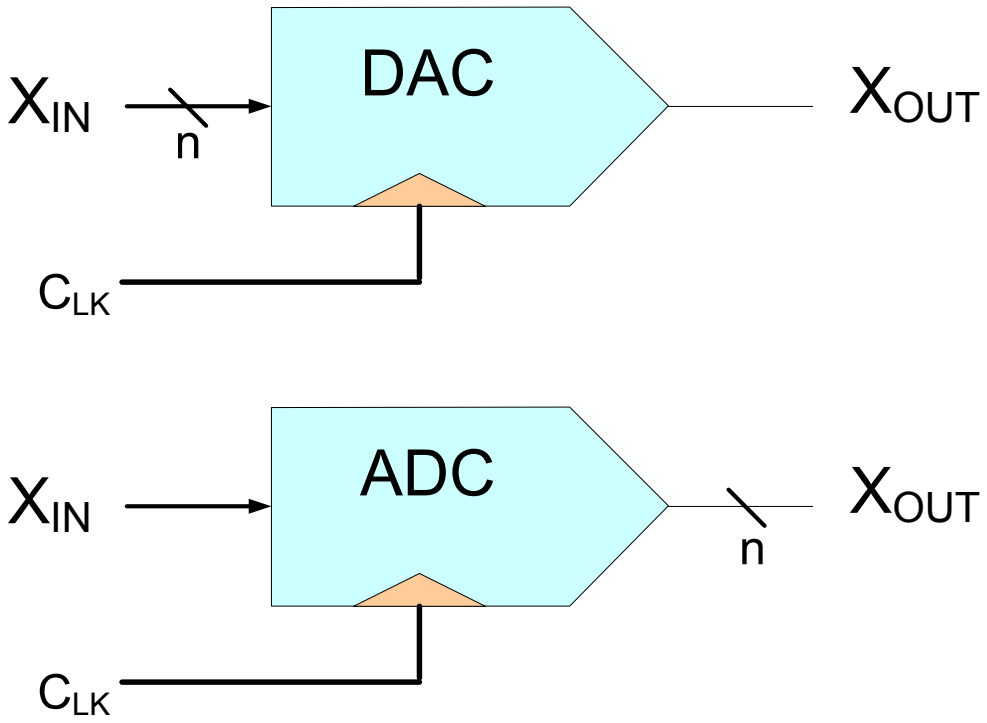
What is an acceptable DNL of a DAC?

If DNL<0.5LSB, it is generally considered acceptable

What is the INL of a DAC?

Varies from part to part, often close to 0.5LSB, occasionally better, but often worse - Given in Data Sheet

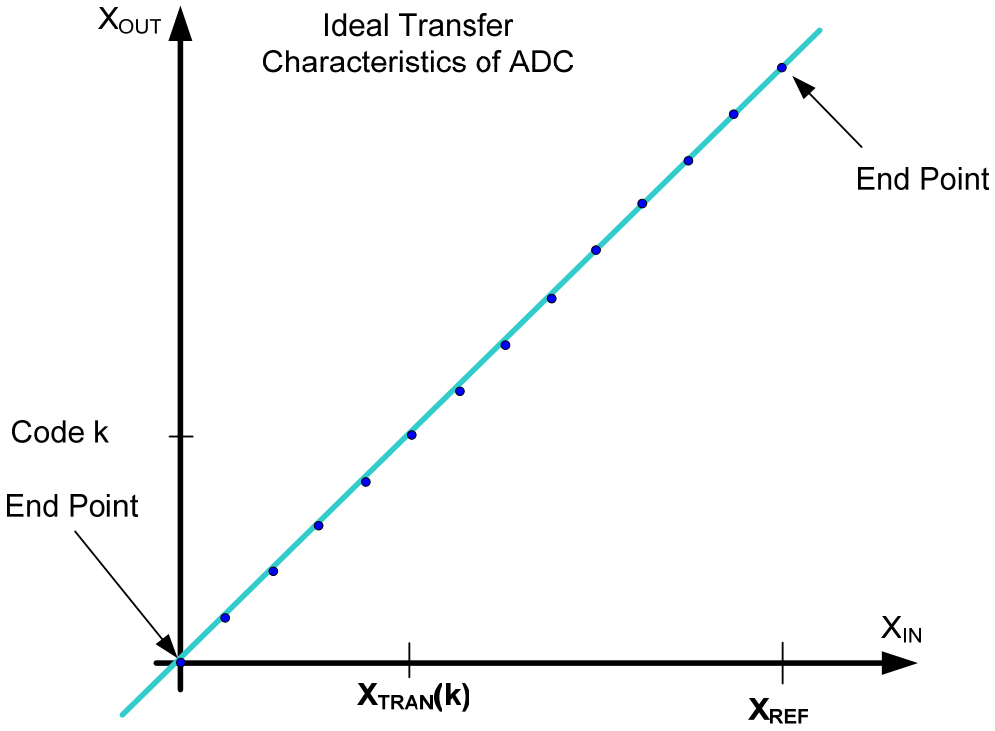
Characterization of Nonlinearities



Linearity metrics:
- INL
- DNL
- THD
- SFDR

Linearity Metrics for ADC and DAC are Analogous to Each Other

Integral Nonlinearity (INL)



Linearity metrics:

- INL
- DNL
- THD
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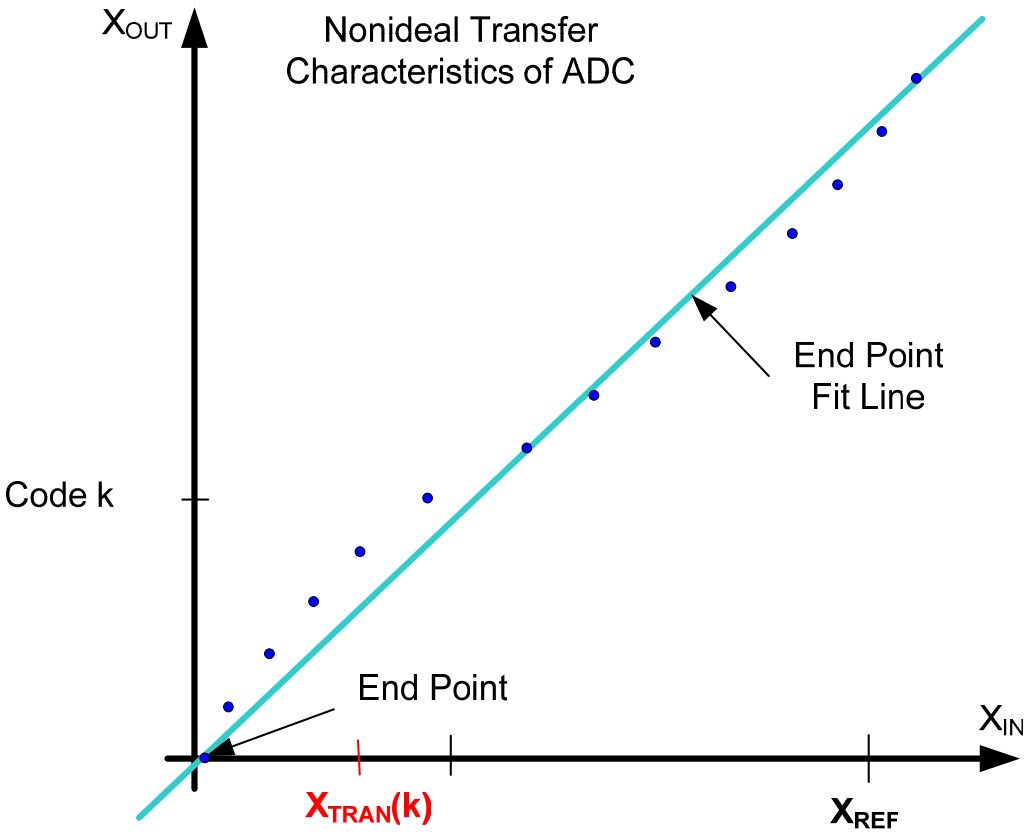
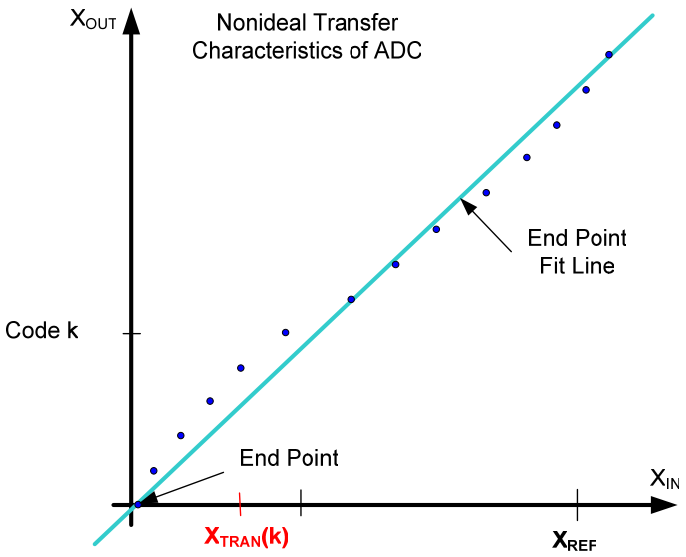
Integral Nonlinearity (INL)

Linearity metrics:
- INL
- DNL
- THD
- SFDR



Integral Nonlinearity (INL)

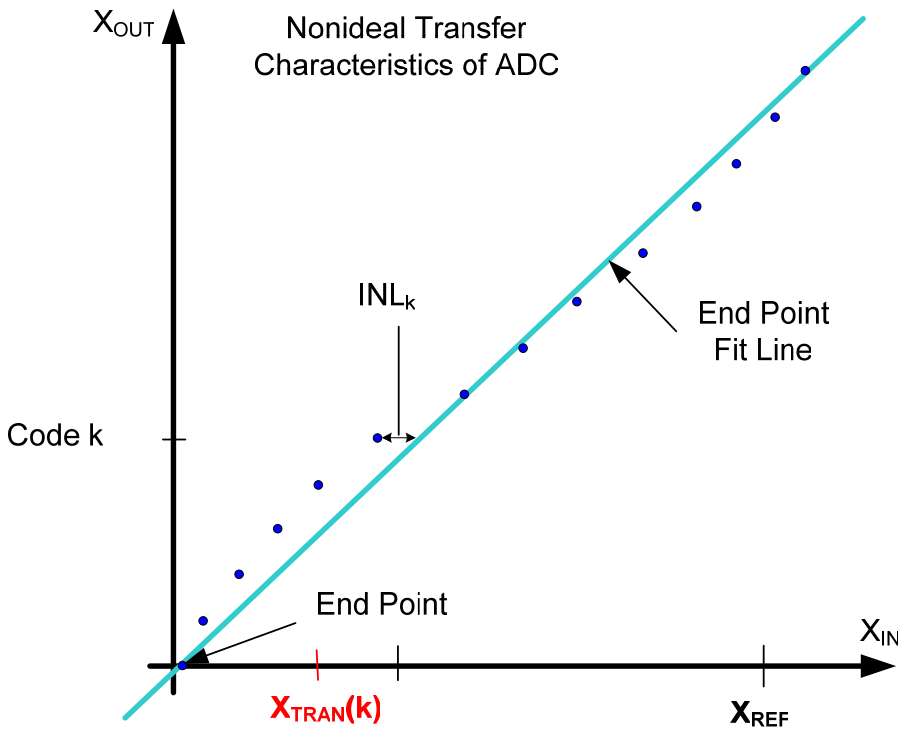


Linearity metrics:
- INL
- DNL
- THD
- SFDR

What is the "gain" of an ideal ADC or an ideal DAC?

- Can think of the gain as being ideally equal to 1
- Thus the horizontal and vertical deviations from a fit line are about the same
- For an ADC, vertical distance not defined AT transition points, horizontal distance only defined AT transition points

Integral Nonlinearity (INL)

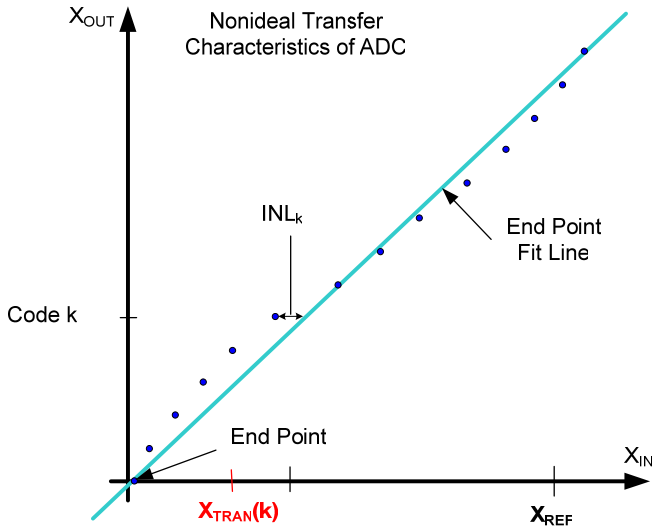


Linearity metrics:
- INL
- DNL
- THD
- SFDR

$$INL_k = X_{TRAN}(k) - X_{FIT}(k)$$

$$X_{FIT}(k) = X_{TRAN}(1) + \left(\frac{k-1}{N-2}\right)\left[X_{TRAN}(N-1) - X_{TRAN}(1)\right]$$

Integral Nonlinearity (INL)



Linearity metrics:
- INL
- DNL
- THD
- SFDR

$$INL_k = X_{TRAN}(k) - X_{FIT}(k)$$

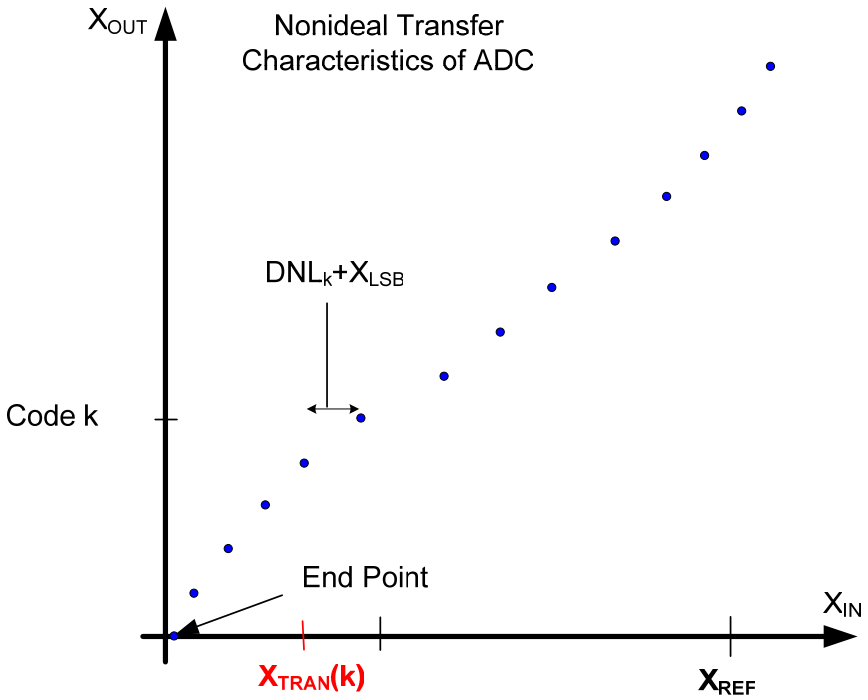
$$INL = \max_{1 \le k \le N} \{ |INL_k| \}$$

$$INL_{LSB} = \frac{INL}{X_{LSBF}}$$

$$INL_{LSB} \cong 2^n \frac{INL}{X_{REF}}$$

INL of an ideal ADC is 0

Differential Nonlinearity (DNL)



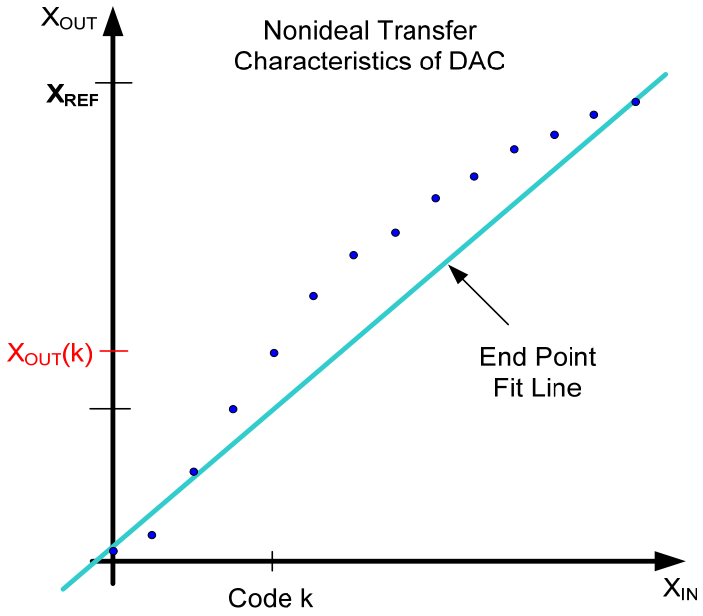
Linearity metrics:

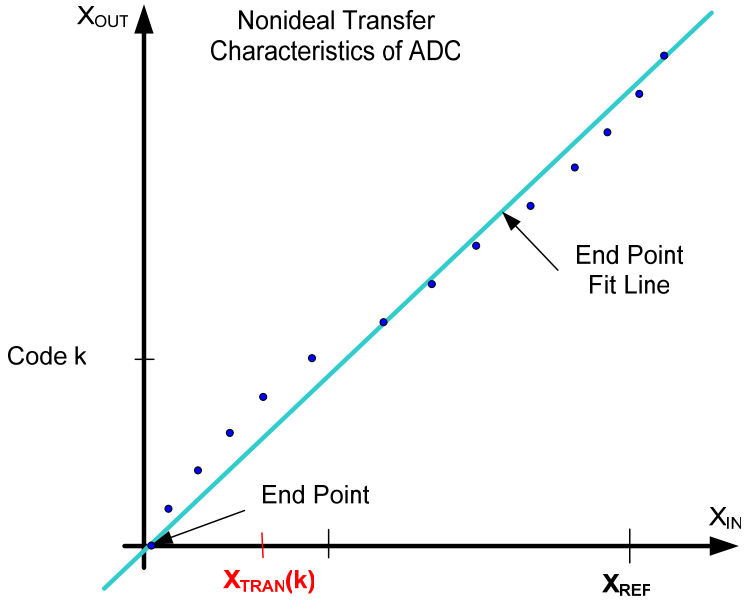
- INL
- DNL
- THD
- SFDR

$$DNL_k \cong X_{TRANS}(k)-X_{TRANS}(k-1)-X_{LSB}$$

$$DNL = \max_{1<k\leq N}\left\{\left|DNL_k\right|\right\}$$

Equivalent Number of Bits -ENOB (based upon linearity)





Generally expect INL to be less than ½ LSB

If INL larger than ½ LSB, effective resolution is less than specified resolution

Equivalent Number of Bits -ENOB (based upon linearity)

Consider initially the continuous INL definition for an ADC where the INL of an ideal ADC is $X_{LSB}/2$

Assume $$INL = \theta X_{REF} = \upsilon X_{LSBR} = \upsilon \frac{X_{REF}}{2^n}$$

where X_{LSBR} is the LSB based upon the defined resolution, n.

Thus $$\theta = \frac{\upsilon}{2^n}$$

Define the LSB by $$x_{LSB} = \frac{x_{REF}}{2^{n_{EQ}}}$$

Thus $$INL = \theta 2^{n_{EQ}} X_{LSB}$$

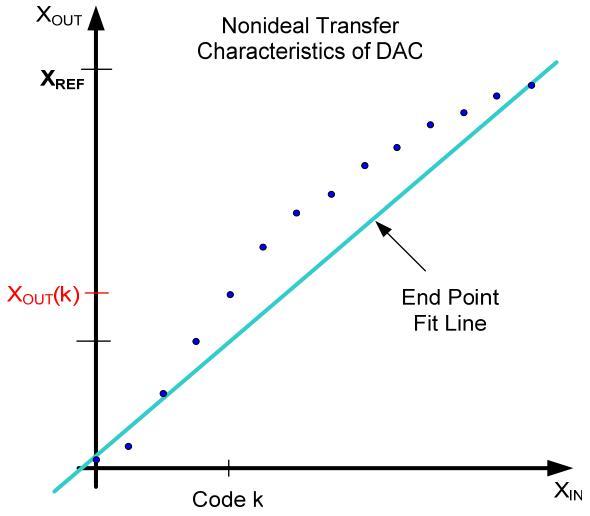
Since an ideal ADC has an INL of $X_{LSB}/2$, express INL in terms of ideal ADC

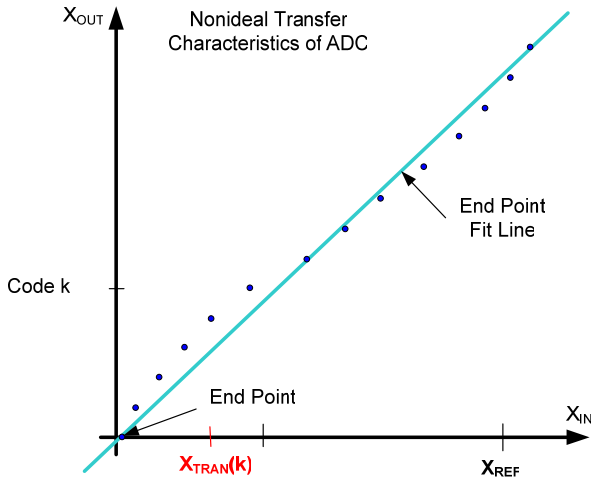
$$INL = \left[\theta 2^{(n_{EQ}+1)}\right]\left(\frac{X_{LSB}}{2}\right)$$

Setting term in [ ] to 1, and substituting for θ, can solve for n_{EQ} to obtain

$$ENOB = n_{EQ} = \log_2\left(\frac{1}{2\theta}\right) = n\text{-}1\text{-}\frac{\log(\upsilon)}{\log(2)}$$

Equivalent Number of Bits -ENOB (based upon linearity)





If v is the INL in LSB

$$ENOB = n\text{-}1 - \frac{\log_{10} v}{\log_{10} 2}$$

v	res
0.5	n
1	n-1
2	n-2
4	n-3
8	n-4
16	n-5

National Semiconductor

May 1999

DAC0808
8-Bit D/A Converter

General Description

The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 $I_{REF}/256$. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 µA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 is independent of bit codes, and exhibits essen

Features

- Relative accuracy: ±0.19% error maximum
- Full scale current match: ±1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/µs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 4)	1000 mW
ESD Susceptibility (Note 5)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808	$0 \le T_A \le +75°C$

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, V_{REF}/R14 = 2 mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	(*Figure 4*)				%
	DAC0808LC (LM1408-8)				**±0.19**	%
	Settling Time to Within ½ LSB (Includes t_{PLH})	T_A=25°C (Note 7), (*Figure 5*)		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, (*Figure 5*)		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	Digital Input Logic Levels	(*Figure 3*)				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}

2.5 V to 5.5 V, 400 µA, 2-Wire Interface, Quad Voltage Output, 8-/10-/12-Bit DACs

AD5306/AD5316/AD5326

FEATURES

- AD5306: 4 buffered, 8-bit DACs in 16-lead TSSOP
- A version: ±1 LSB INL; B version: ±0.625 LSB INL
- AD5316: 4 buffered, 10-bit DACs in 16-lead TSSOP
- A version: ±4 LSB INL; B version: ±2.5 LSB INL
- AD5326: 4 buffered, 12-bit DACs in 16-lead TSSOP
- A version: ±16 LSB INL; B version: ±10 LSB INL
- Low power operation: 400 µA @ 3 V, 500 µA @ 5 V
- 2-wire (I^2C®-compatible) serial interface
- 2.5 V to 5.5 V power supply
- Guaranteed monotonic by design over all codes
- Power-down to 90 nA @ 3 V, 300 nA @ 5 V ($\overline{PD}$ pin or bit)
- Double-buffered input logic
- Buffered/unbuffered reference input options
- Output range: 0 V to V_{REF} or 0 V to 2 V_{REF}
- Power-on reset to 0 V
- Simultaneous update of outputs ($\overline{LDAC}$ pin)

FUNCTIONAL BLOCK DIAGRAM

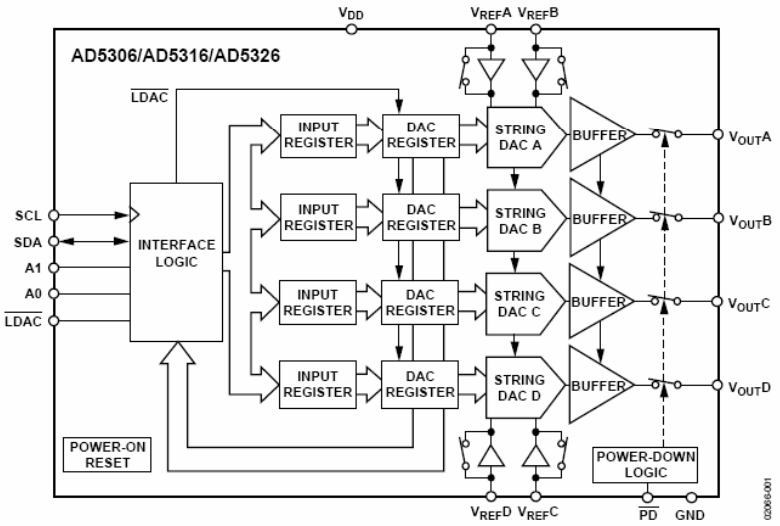


Figure 1.

SPECIFICATIONS

V_{DD} = 2.5 V to 5.5 V; V_{REF} = 2 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

	A Version[1]			B Version[1]				
Parameter[2]	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
DC PERFORMANCE[3, 4]								
AD5306								
Resolution		8			8		Bits	
Relative Accuracy		±0.15	±1		±0.15	±0.625	LSB	
Differential Nonlinearity		±0.02	±0.25		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes.
AD5316								
Resolution		10			10		Bits	
Relative Accuracy		±0.5	±4		±0.5	±2.5	LSB	
Differential Nonlinearity		±0.05	±0.5		±0.05	±0.5	LSB	Guaranteed monotonic by design over all codes.
AD5326								
Resolution		12			12		Bits	
Relative Accuracy		±2	±16		±2	±10	LSB	
Differential Nonlinearity		±0.2	±1		±0.2	±1	LSB	Guaranteed monotonic by design over all codes.
Offset Error		±5	±60		±5	±60	mV	V_{DD} = 4.5 V, gain = 2; see Figure 4 and Figure 5.
Gain Error		±0.3	±1.25		±0.3	±1.25	% of FSR	V_{DD} = 4.5 V, gain = 2; see Figure 4 and Figure 5.

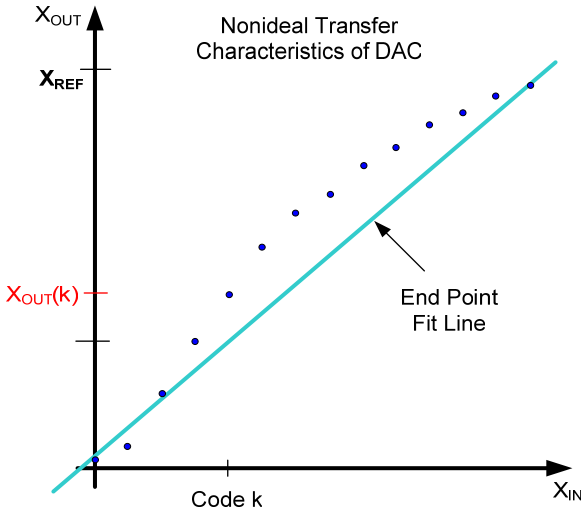
AC CHARACTERISTICS

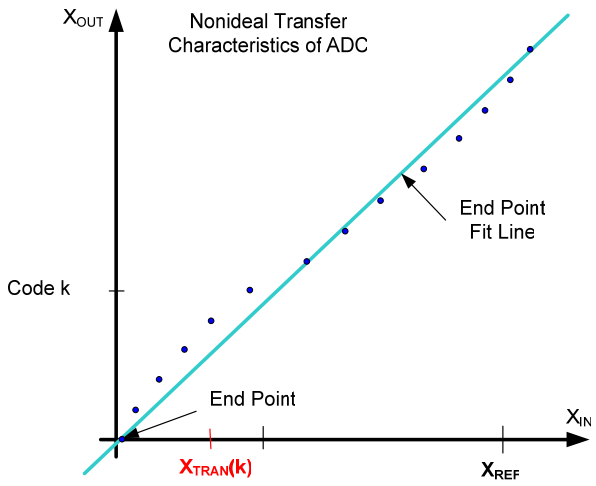
V_{DD} = 2.5 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	A, B Versions[1, 2]				
Parameter[3]	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
Output Voltage Settling Time					V_{REF} = V_{DD} = 5 V
AD5306		6	8	µs	1/4 scale to 3/4 scale change (0x40 to 0xC0)
AD5316		7	9	µs	1/4 scale to 3/4 scale change (0x100 to 0x300)
AD5326		8	10	µs	1/4 scale to 3/4 scale change (0x400 to 0xC00)
Slew Rate		0.7		V/µs	
Major-Code Change Glitch Energy		12		nV-s	1 LSB change around major carry
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		0.5		nV-s	
Analog Crosstalk		1		nV-s	
DAC-to-DAC Crosstalk		3		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ± 0.1 V p-p, unbuffered mode
Total Harmonic Distortion		−70		dB	V_{REF} = 2.5 V ± 0.1 V p-p, frequency = 10 kHz

Spectral Characterization





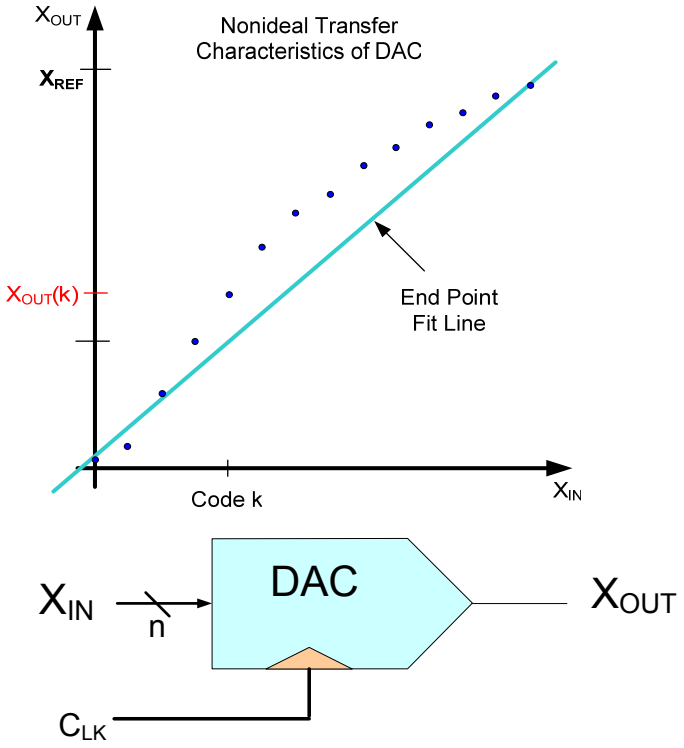
Linearity metrics:

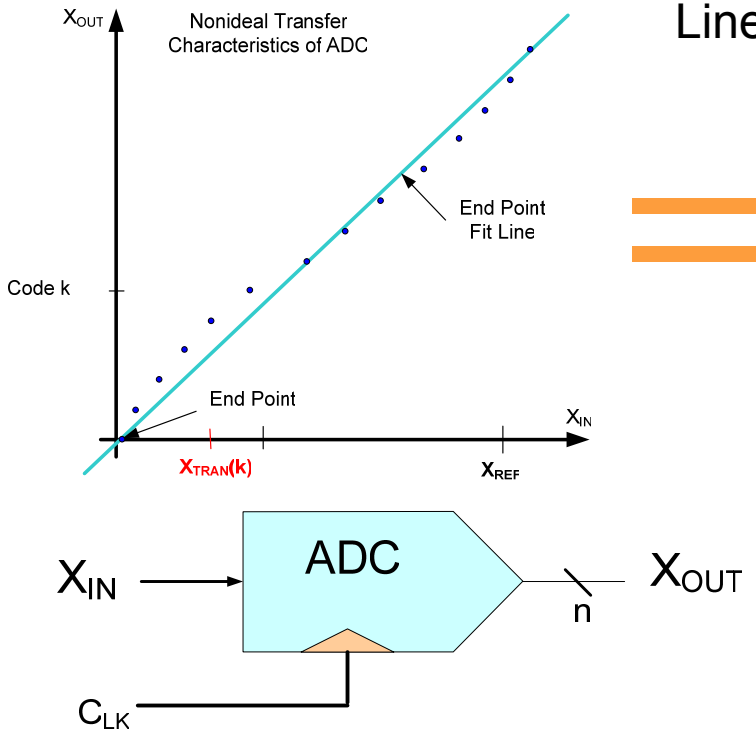
- INL
- DNL
- THD
- SFDR

INL and DNL do not give a good indicator of linearity of a data converter in some (many) applications

THD and SFDR are alternate ways to characterize the linearity of a data converter

Spectral Characterization





Linearity metrics:

- INL
- DNL
- THD
- SFDR

$$X_{IN} = X_M \sin(\omega t + \theta)$$

If nonlinearities present, X_{OUT} given by

$$X_{OUT} = A_0 + A_1 \sin(\omega t + \theta + \gamma_1) + \sum_{k=2}^{\infty} A_k \sin(k\omega t + \theta + \gamma_k)$$

Spectral Characterization

$$X_{IN}=X_M\sin(\omega t+\theta)$$

$$X_{OUT}=A_0+A_1\sin(\omega t+\theta+\gamma_1)+\sum_{k=2}^{\infty}A_k\sin(k\omega t+\theta+\gamma_k)$$

A_k, k>1 are all spectral distortion components

Generally only first few terms are large enough to represent significant distortion

$$THD=\frac{\sum_{k=2}^{\infty}A_k^2}{A_1^2}$$

$$THD_{dB}=10\log_{10}\left(\frac{\sum_{k=2}^{\infty}A_k^2}{A_1^2}\right)$$

$$SFDR=\frac{|A_1|}{\max_{1<k}\{|A_k|\}}$$

$$SFDR_{dB}=20\log_{10}\left(\frac{|A_1|}{\max_{1<k}\{|A_k|\}}\right)$$

Spectral Characterization

$$X_{IN} = X_M \sin(\omega t + \theta)$$

$$X_{OUT} = A_0 + A_1 \sin(\omega t + \theta + \gamma_1) + \sum_{k=2}^{\infty} A_k \sin(k\omega t + \theta + \gamma_k)$$

Generally X_M is chosen nearly full-scale and input is offset by $X_{REF}/2$

$$X_{IN} = \frac{X_{REF}}{2} + \left(\frac{X_{REF}}{2} - \varepsilon \right) \sin(\omega t + \theta)$$

Direct measurement of A_k terms not feasible

A_k generally calculated from a large number of samples of $X_{OUT}(t)$

Spectral Characterization

$$X_{IN} = X_M \sin(\omega t + \theta)$$

$$X_{OUT} = A_0 + A_1 \sin(\omega t + \theta + \gamma_1) + \sum_{k=2}^{\infty} A_k \sin(k\omega t + \theta + \gamma_k)$$

Key theorem useful for spectral characterization

Theorem: If a periodic signal x(t) with period T=1/f is band-limited to frequency hf and if the signal is sampled N times over an integral number of periods, N_P, then

$$|A_m| = \frac{2}{N} |X(mN_P + 1)| \qquad \text{for } 0 \le m \le h\text{-}1$$

where $\langle X(k) \rangle_{k=1}^{N-1}$ **is the DFT of the sampled sequence** $\langle x(kT_S) \rangle_{k=1}^{N-1}$ **where T_S is the sampling period.**

$$T_S = \frac{T \bullet N_P}{N}$$

Spectral Characterization

$$X_{IN} = X_M \sin(\omega t + \theta)$$

$$X_{OUT} = A_0 + A_1 \sin(\omega t + \theta + \gamma_1) + \sum_{k=2}^{\infty} A_k \sin(k\omega t + \theta + \gamma_k)$$

Key theorem useful for spectral characterization

Theorem: If a periodic signal x(t) with period T=1/f is band-limited to frequency hf and if the signal is sampled N times over an integral number of periods, N_P, then

$$|A_m| = \frac{2}{N} |X(mN_P + 1)| \qquad \text{for } 0 \le m \le h\text{-}1$$

where $\langle X(k) \rangle_{k=1}^{N-1}$ **is the DFT of the sampled sequence** $\langle x(kT_S) \rangle_{k=1}^{N-1}$ **where T_S is the sampling period.**

- This theorem is usually not stated although widely used
- Often this theorem is misunderstood or misused
- If hypothesis not exactly satisfied, major problems with trying to use this theorem

Spectral Characterization

$$X_{IN} = X_M \sin(\omega t + \theta)$$

$$X_{OUT} = A_0 + A_1 \sin(\omega t + \theta + \gamma_1) + \sum_{k=2}^{\infty} A_k \sin(k\omega t + \theta + \gamma_k)$$

Key theorem useful for spectral characterization

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Spectral Characterization

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where $\langle X(k)\rangle_{k=1}^{N-1}$ **is the DFT of the sampled sequence** $\langle x(kT_S)\rangle_{k=1}^{N-1}$ **where T_S is the sampling period.**

- Usually N_p is a prime number (e.g. 11, 21, 29, 31)
- If N is a power of 2, the Fast Fourier Transform (FFT) is a computationally efficient method for calculating the DFT
- Often N=4096, 65,536, …
- FFT is available in Matlab and as subroutines for C++

Spectral Characterization

Key theorem useful for spectral characterization

Theorem: If a periodic signal x(t) with period T=1/f is band-limited to frequency hf and if the signal is sampled N times over an integral number of periods, N_P, then

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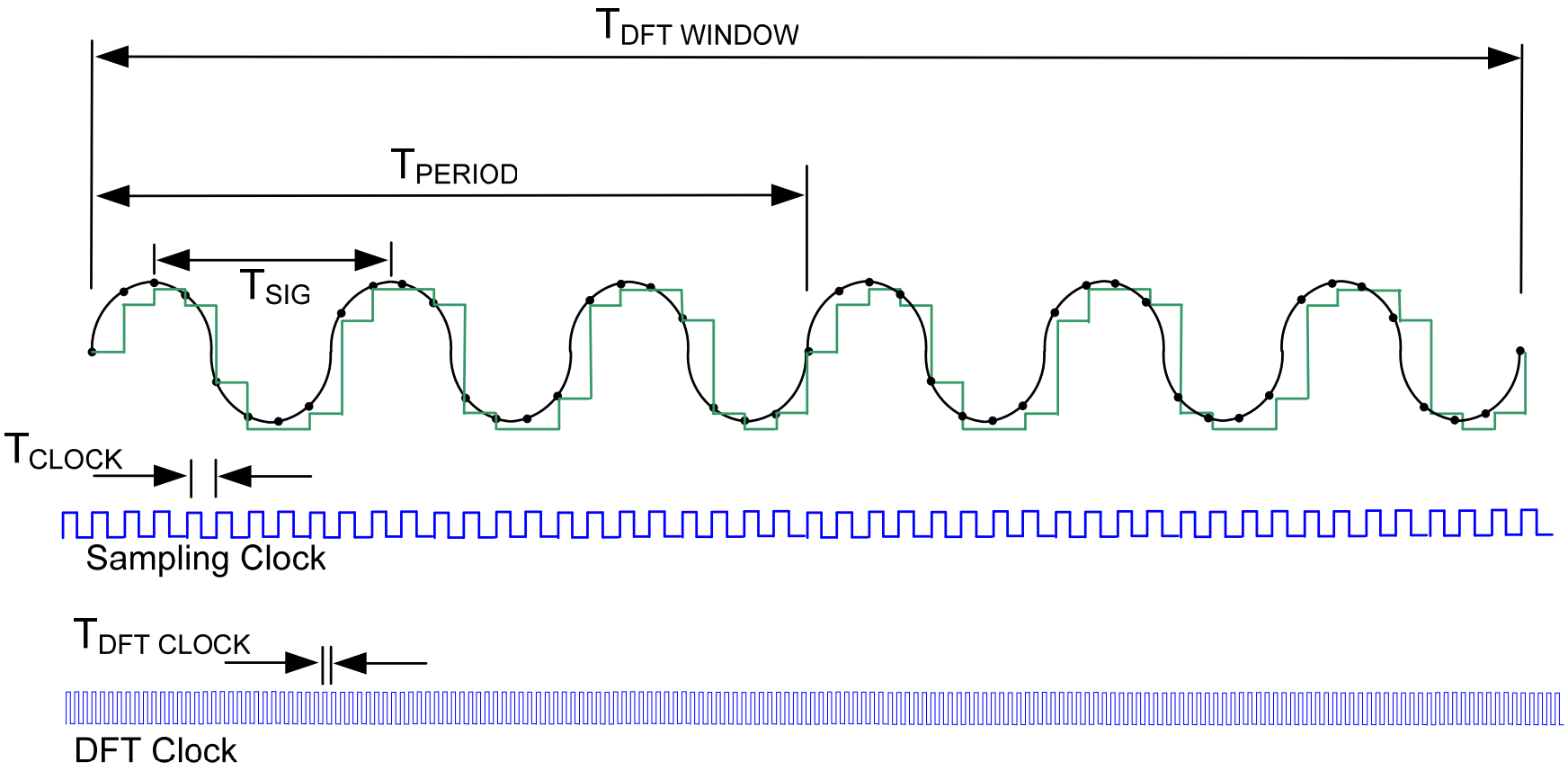
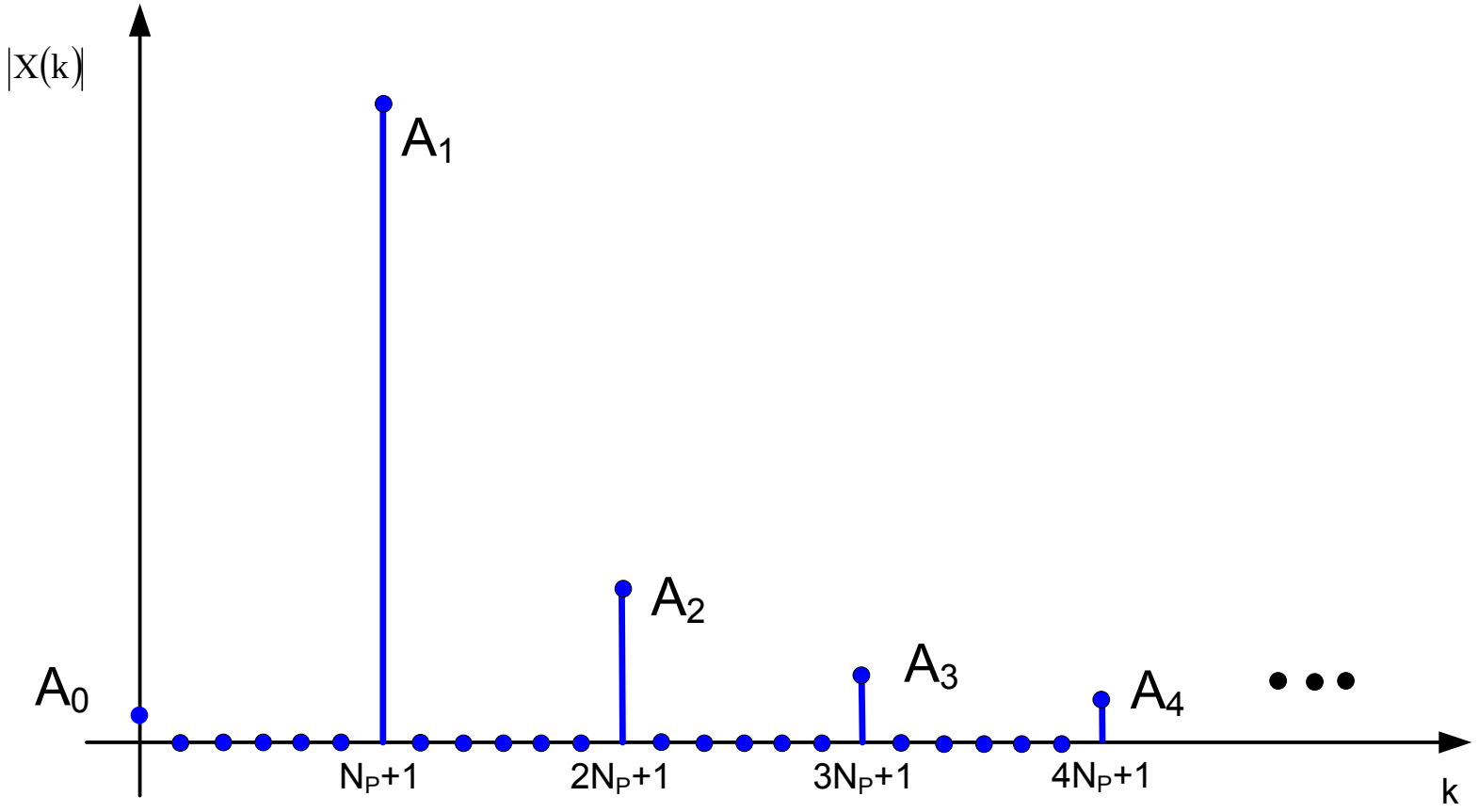
where $\langle X(k)\rangle_{k=1}^{N-1}$ **is the DFT of the sampled sequence** $\langle x(kT_S)\rangle_{k=1}^{N-1}$ **where T_S is the sampling period.**

$A_0, A_1, A_2, A_3, \ldots$ are the magnitudes of the DFT elements $X(0)$, $X(N_P+1)$, $X(2N_P+1)$, $X(3N_P+1)$, … respectively

Spectral Characterization



Spectral Characterization



Example

Determine the resolution of an ideal data converter needed for an electronic scale that can be used for weighing commodities at a grain elevator in Iowa that has a total scale capacity of 50 tons. Assume the scale is an electronic scale with a load cell whose output goes to a single ADC.

Additional information:

The State of Iowa stipulates that scales must be accurate to within ±0.1% of full scale

Solution:

The accuracy requirement corresponds to ½ LSB. If 100% is full scale, then ½ LSB=0.1%, thus 1LSB=0.2% So, the resolution n must satisfy the relationship

$$X_{LSB} = \frac{X_{REF}}{2^n}$$

$$0.2\% = \frac{100\%}{2^n}$$

$$n = \frac{\log_{10}(500)}{\log_{10}(2)} = 8.96 \quad \Rightarrow \quad n=9$$

Example

If the data converter is 9 bits,

i. what is the worst-case error in the measurement of 50 bushels of corn on this scale

a) in pounds

b) In bushels

c) in %?

Ii If the market price of corn is $3.50/bu, what is the worst-case financial impact of this error?

Solution:

Let e be the maximum error.

i.

$$e_{LBS} = \frac{50tons \bullet \frac{2000lbs}{ton}}{2^9} = \frac{100,000lbs}{512} = 195lbs$$

$$e_{BU} = 195lbs \bullet \frac{1bu}{56lbs} = 3.48bu$$

$$e_{PCT} = \frac{3.48bu}{50bu} \bullet 100\% = 6.9\%$$

Example

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Ii If the market price of corn is $3.50/bu, what is the worst-case financial impact of this error?

Solution:

Let e be the maximum error.

ii.

$$e_{Dollars} = 3.48bu \bullet \frac{\$3.50}{bu} = \$12.20$$

End of Lecture 43